AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED REVISION TO 37 CFR 1.121)

Please cancel claims 17-20 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to present a parallel output data signal in response to (i) a first clock signal and (ii) ~~one~~ two or more serial data signals; and

a second circuit configured to present said ~~one~~ two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

2. (ORIGINAL) The apparatus according to claim 1, wherein said first clock signal comprises a bit clock signal.

3. (ORIGINAL) The apparatus according to claim 1, wherein said second clock signal comprises a reference clock signal.

4. (ORIGINAL) The apparatus according to claim 1, wherein said first circuit further comprises:

a third circuit configured to generate (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

5. (CURRENTLY AMENDED) The apparatus according to claim 4, wherein said first circuit further comprises:

a phase comparator circuit configured to generate said phase select signal in response to said one or more select signals and ~~one~~ a first of said ~~one~~ two or more serial data signals.

6. (ORIGINAL) The apparatus according to claim 4, wherein said third circuit comprises a phase generation and select circuit.

7. (CURRENTLY AMENDED) The apparatus according to claim ~~4~~ 5, wherein said first circuit includes a deserializer circuit configured to generate said parallel output data signal in response to said selected clock signal and ~~another one~~ a second of said ~~one~~ two or more serial data signals.

8. (CURRENTLY AMENDED) The apparatus according to claim 7, wherein said first circuit further comprises:

a multiplexer configured to generate (i) said ~~one of~~ first of said ~~one~~ two or more serial data signals and (ii) said

~~another one~~ second of said ~~one~~ two or more serial data signals, in response to said ~~one~~ two or more serial data signals.

9. (CURRENTLY AMENDED) A circuit comprising:

means for generating a parallel output data signal in response to (i) a first clock signal and (ii) ~~one~~ two or more serial data signals; and

means for generating said ~~one~~ two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

10. (CURRENTLY AMENDED) A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

(A) generating a parallel output data signal in response to (i) a first clock signal and (ii) ~~one~~ two or more serial data signals; and

(B) generating said ~~one~~ two or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal, wherein said first clock signal is configured to control said pulse width.

11. (ORIGINAL) The method according to claim 10, wherein said first clock signal comprises a bit clock signal.

12. (ORIGINAL) The method according to claim 10, wherein said second clock signal comprises a reference clock signal.

13. (ORIGINAL) The method according to claim 10, wherein step (A) further comprises the sub-step of:

generating (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

14. (CURRENTLY AMENDED) The method according to claim 13, wherein step (A) further comprises the sub-step of:

generating said phase select signal in response to said one or more select signals and ~~one~~ a first of said ~~one~~ two or more serial data signals.

15. (CURRENTLY AMENDED) The method according to claim 14, wherein step (A) further comprises the sub-step of:

generating said parallel output data signal in response to said selected clock signal and ~~another one~~ a second of said ~~one~~ two or more serial data signals.

16. (CURRENTLY AMENDED) The method according to claim 15, further comprising the step of:

generating said ~~one~~ first of said ~~one~~ two or more serial data signals and said ~~another one~~ second of said ~~one~~ two or more serial data signals, in response to said ~~one~~ two or more serial data signals.

17. (CANCEL)

18. (CANCEL)

19. (CANCEL)

20. (CANCEL)